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Observation of trap-related phenomena in electrical performance of back-gated MoS_2 field-effect transistors

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Abstract

Trap-related phenomena in the electrical performance of back-gated mechanical exfoliated MoS_2 field-effect transistors are investigated in terms of the super linear increase in the drain current under positive gate bias and the shift of transfer curves with gate voltage stress. The super linear increase in drain current is only observed for the MoS_2 field-effect transistors in the electron accumulation regime under positive gate bias, which can be attributed to a trap-assisted tunneling effect with S vacancies at the contact interface between metal Ti and MoS_2. After thermal annealing of the devices in vacuum at 300 °C for 2 h, the almost complete metallization of Ti contacting with the MoS_2 layer leads to the variation of the drain current relationship with drain voltage from a super linear to a linear increase, thus screening the efficacy of the mechanism of defect level assisted electron tunneling. The shift of transfer curves with gate voltage stress (denoted as hysteresis) is attributed to the defects near the interface between MoS_2 and SiO_2, which is slightly impacted by thermal annealing. The hump effect caused by parasitic transistors is also observed in back-gated mechanical exfoliated MoS_2 field-effect transistors. These results further enrich the knowledge of the complex electrical characteristics of MoS_2 field-effect transistors.

Supplementary material for this article is available online

Keywords: MoS_2, field effect transistors, defect traps, hysteresis

(Some figures may appear in colour only in the online journal)

1. Introduction

Molybdenum disulfide (MoS_2), a representative 2D semiconductor with a band gap of 1.2 eV for bulk and of 1.8 eV for monolayer [1, 2], has attracted tremendous interest due to its potential applications in microelectronics and optoelectronics [3, 4]. Several superiorities of 2D MoS_2 compared with those of traditional semiconductors, such as low-surface scattering [5], superior immunity to short channel effects [6] and large density of states [7], make it more promising for future field-effect transistors (FETs). Thus, considerable effort has been devoted to the fabrication and characterization of MoS_2 FETs, which reveals superior performance such as high on/off ratio (10^8), steep subthreshold swing (74 mV dec^{-1}) and considerable mobility (517 $cm^2\ V^{-1}\ s^{-1}$) [8, 9].

However, to realize high performance MoS_2 FETs, there are still several scientific issues that need further study. The quality of MoS_2 is one of the most important aspects to determine the performance of MoS_2 FETs. Although the quality of exfoliated MoS_2 is usually better than that of chemical vapor deposition-growth MoS_2, there are still defect levels due to S vacancies on the surface of MoS_2 flakes [10–14]. Due to stronger electronegativity of S atoms in the MoS_2 crystal, S vacancies which form defect levels near the bottom

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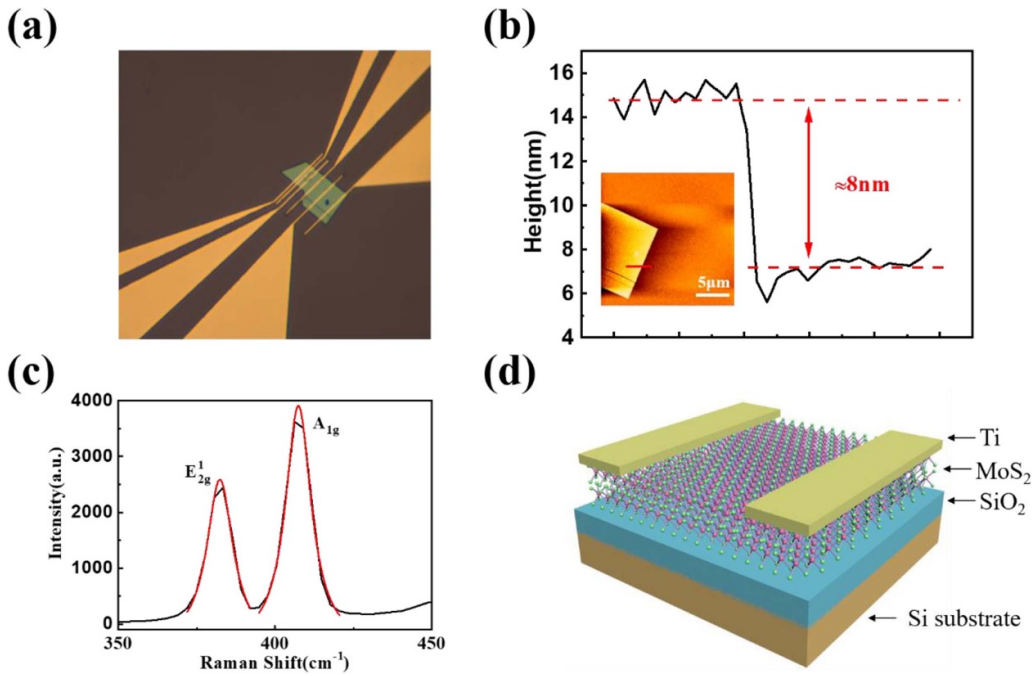

Figure 1. (a) An optical microscope diagram of the TLM structure. (b) The thickness of the MoS_2 flake. The inset shows the atomic force microscope image of the MoS_2 flake. (c) The Raman spectra of the MoS_2 flake. (d) The 3D schematic view of a back-gated MoS_2 FET.

of conduction bands in MoS_2 reveal donor behavior [10]. S vacancies are the dominant point defects in mechanical exfoliated samples, with a surface density of 10^{13} cm^{-2} [13]. Moreover, the dielectric environment has a great effect on some of the parameters of devices directly, such as mobility and the subthreshold swing. Although much effort has been made to improve the dielectric environment of 2D material devices, the appearance of hysteresis in MoS_2 FETs is still not removed effectively and even the explaination of the mechanism is under debate [15–18]. Although no discussion has been presented, the super linear increase in the drain current in the output characteristics in some ranges of drain voltage was observed in several groups [19–24]. The mechanisms hidden in the phenomena need further investigation for improvement of the performance of MoS_2 FETs.

In this work, a transfer length method (TLM) structure containing five back-gated FETs with various channel lengths, which can be independently operated, was fabricated. Both the specific contact resistance and sheet resistance of the MoS_2 channel can be extracted from the TLM structure at various gate bias voltages, which delineates the electric properties of the MoS_2 channel at different gate biases for further analysis. The impacts of thermal annealing in vacuum on the output characteristics of back-gated MoS_2 FETs are investigated, in which the super linear increase in the drain current is eliminated. S vacancies are deemed to introduce the super linear increase in the drain current. The complete metallization of Ti contacting with the MoS_2 layer may be responsible for eliminating the super linear increase after annealing. The hysteresis effects in transfer curves of MoS_2 FETs are also studied with different gate voltage sweep ranges, and the origin of hysteresis is also discussed.

2. Experiment

A TLM structure containing five back-gated MoS_2 FETs with various channel lengths was fabricated by electron beam lithography techniques. The channel lengths of the five back-gated MoS_2 FETs are 0.5 μm, 1 μm, 2 μm, 3 μm and 4 μm, respectively, spaced by 0.5 μm wide Ti contact electrodes. The five devices are fabricated on the same piece of MoS_2 flake so that their properties can be compared directly without considering the variation of the flake thickness, surface defects and carrier density. An optical microscope diagram of the TLM structure is shown in figure 1(a). The MoS_2 flakes were mechanically exfoliated using Scotch tape from bulk MoS_2 and transferred to a surface of 90 nm SiO_2 covering a heavily doped p-type Si substrate. The thickness of the MoS_2 flake we chose is 8 nm, corresponding to 12 layers, as shown in figure 1(b). The interval of Raman characteristic peaks between $E^1{}_{2g}$ and A_{1g} is about 25 cm^{-1}, as shown in figure 1(c), indicating that the number of layers of the MoS_2 flake is more than six [25].

Polymethyl methacrylate was spun on the surface of the MoS_2 flake followed by definition of the pattern of the electrodes by electron beam lithography. Then, 50 nm thick Ti was deposited on the sample by magnetron sputtering. The lift-off process was performed in 50 °C hot acetone to define the Ti electrodes. Finally, 300 nm thick Al was deposited on the back-side of Si as the gate electrode. The 3D schematic of the back-gated MoS_2 FET is shown in figure 1(d). After measurements of the transfer curves and output characteristics, the TLM structure was thermally annealed at 300 °C in vacuum for 2 h to eliminate adsorbates on the MoS_2 surface and improve the quality of the contact interface between Ti and

MoS_2. All the electrical measurements were performed on the Keithley 4200 at room temperature in a dark box.

3. Results and discussion

To understand the carrier transport in the MoS_2 channel, the specific contact resistance and sheet resistance are extracted from the TLM structures under various gate voltages. Because the width of the MoS_2 flake is not uniform, the measured current densities are normalized by the contact length for comparison. The TLM model is described as the equation [26]:

$$R_{\text{Total}} = R_{\text{sh}} \cdot (L/W) + 2R_{\text{C}}$$
$$= R_{\text{sh}} \cdot (L + 2L_T)/W$$

where R_{sh} is the square resistance, and L and W are the length and width of the MoS_2 channel, respectively. The R_{C} is the contact resistance, which is equal to $R_{\text{sh}}L_T/W$, where L_T is the critical length. To facilitate comparison, the equation can be written as $R_{\text{Total}} \cdot W = R_{\text{sh}} \cdot (L + 2L_T)$, where R_{sh} is the slope of this function, and $2R_{\text{sh}}L_T$ is the intercept on the x-axis of this function. With the data of total resistance vs channel length, we can extract the specific contact resistance and sheet resistance of the MoS_2 channel. Figure 2 shows the dependence of the measured total resistance (at a low drain voltage of 0.1 V) on channel length for the TLM structure under various gate bias voltages of −20 V, −10 V, 0 V, 10 V and 20 V, respectively. The total resistance was calculated through the output characteristics, as shown in figure S1 (available online at stacks.iop.org/SST/35/095023/mmedia) of the supporting information and figure 5(a). The specific contact resistance and sheet resistance are extracted from the fitting results and listed in table 1 and are also shown in figure 3. The resistivity of the MoS_2 channel derived from the sheet resistance with thickness is also listed in table 1. It is indicated that the sheet resistance of the MoS_2 flake is controlled by the gate voltage. For the devices under a gate voltage of 20 V, the sheet resistance R_{sh} is about $2.7 \times 10^4\ \Omega\ \square^{-1}$, gradually increasing to $8.9 \times 10^4\ \Omega\ \square^{-1}$ for 0 V gate bias, and sharply increasing to $1.8 \times 10^6\ \Omega\ \square^{-1}$ by two orders of magnitude for −20 V gate bias due to electron depletion in the channel as expected. What is interesting and different from traditional semiconductors is that the contact resistivity also changes as the gate voltage changes. The specific contact resistivity also increases quickly when the MoS_2 is depleted under negative gate bias. These results indicate that gate voltage induced electron accumulation or depletion in the MoS_2 channel cannot only change the electron density in the MoS_2 channel, but also effectively shift its Fermi-level energy and modulate the effective contact barrier height. Due to the ultrathin thickness of the MoS_2 film, the whole flake of the MoS_2 would be influenced sharply by the variation of the gate voltage. The energy band of the MoS_2 moves down as the gate voltage increases. Hence, the depletion width of the MoS_2 caused by the metal-semiconductor contact would be narrower when the gate voltage increases further. This results in the increase in the tunneling current at the contact interface, being presented as the decrease of the effective contact barrier height.

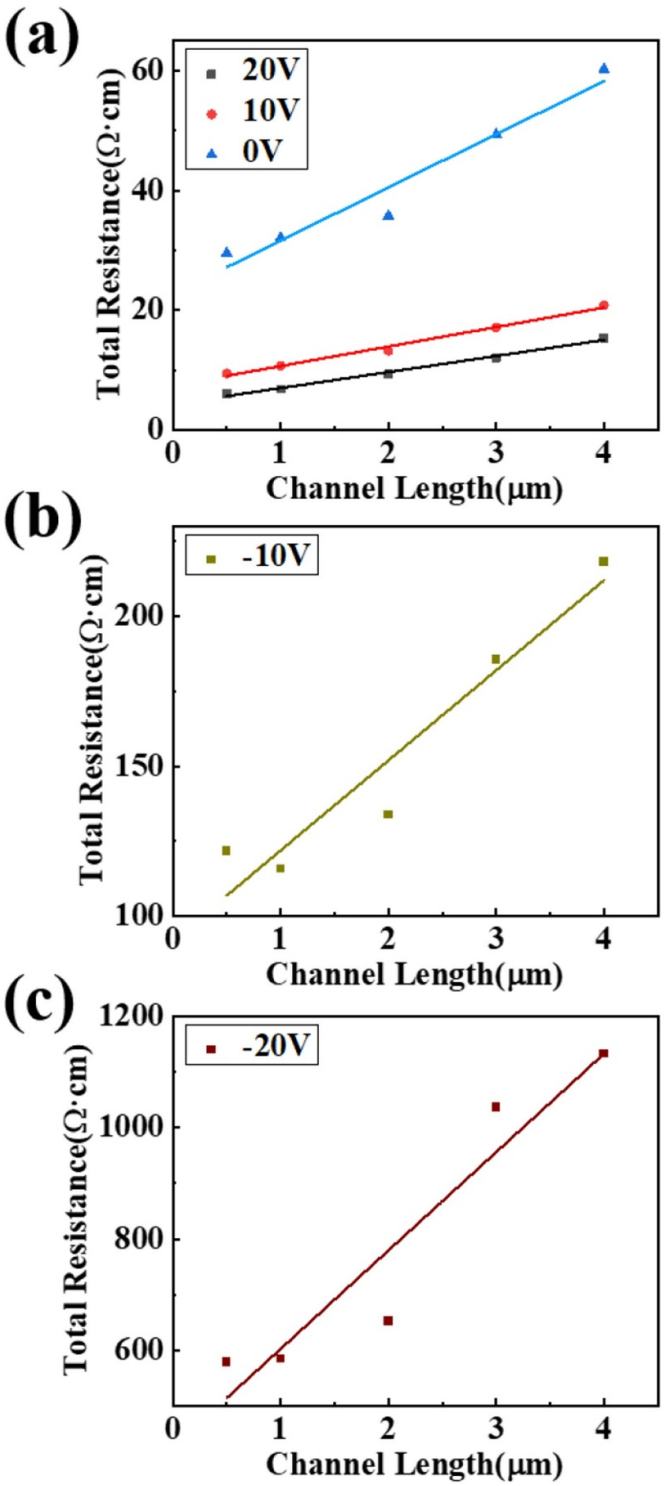

Figure 2. (a) The TLM plot under gate voltages of 20 V, 10 V and 0 V. (b) The TLM plot under a gate voltage of −10 V. (c) The TLM plot under a gate voltage of −20 V.

The electrical characteristics of the back-gated MoS_2 FETs with various channel lengths are measured before and after thermal annealing at 300 °C for 2 h. Figure 4 shows typical I_{ds}–V_{bg} transfer curves of MoS_2 FET with 3 μm channel length under a drain voltage of 0.05 V with both logarithmic (right) and linear (left) coordinates. The I_{ds}–V_{bg} transfer curves of

Table 1. A list of specific contact resistivity, sheet resistance and resistivity of the MoS_2 channel extracted from TLM structures.

	20 V	10 V	0 V	−10 V	−20 V
$\rho_c(\Omega \cdot cm^2)$	2.2×10^{-4}	3.7×10^{-4}	11×10^{-4}	46×10^{-4}	213×10^{-4}
$R_{sh}(\Omega\ \square^{-1})$	2.7×10^{4}	3.3×10^{4}	8.9×10^{4}	30×10^{4}	177×10^{4}
$\rho(\Omega \cdot cm)$	2.16×10^{-2}	2.64×10^{-2}	7.12×10^{-2}	2.4×10^{-1}	9.4×10^{-1}

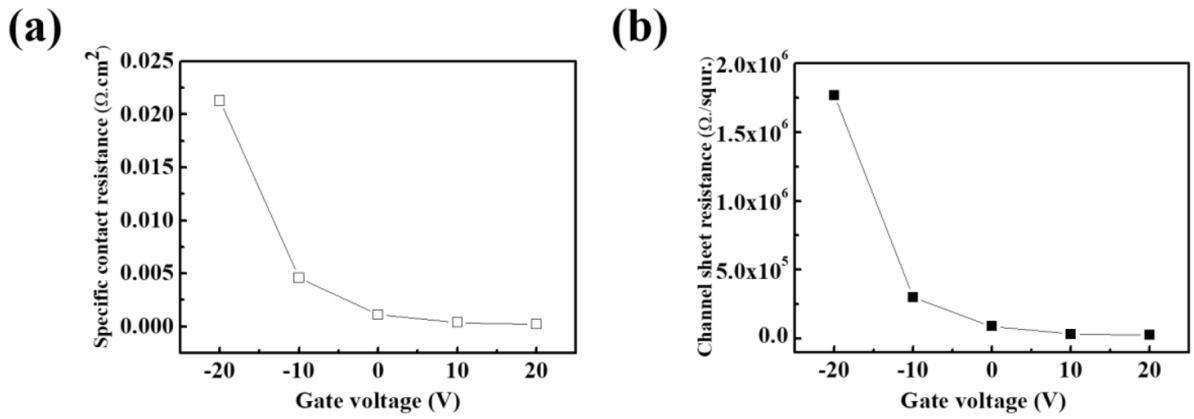

Figure 3. The dependence of contact resistance (a) and sheet resistance (b) on gate bias voltage for the MoS_2 TLM structure.

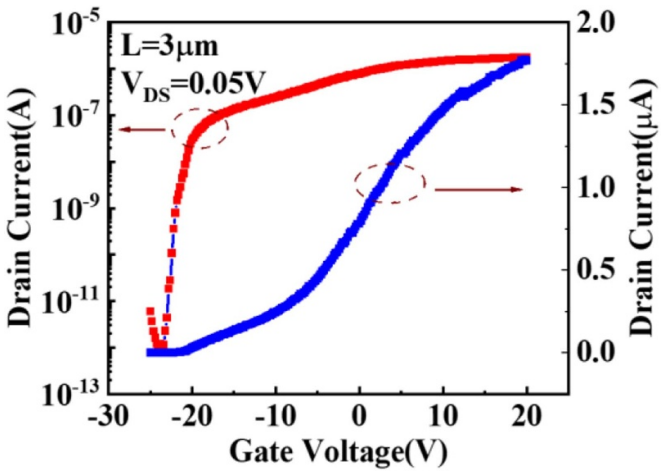

Figure 4. Transfer characteristics of back-gated MoS_2 FET with 3 μm channel length.

MoS_2 FET with 0.5 μm, 1 μm, 2 μm, 4 μm channel lengths under a drain voltage of 0.05 V with both logarithmic (right) and linear (left) coordinates are shown in figure S2 of the supporting information. The drain current on/off ratio of 10^6 is achieved for the MoS_2 FET under the drain-source voltage of 0.05 V. The effective electron mobility of the device can be extracted with the equation $\mu = (dI_{ds}/dV_{bg}) \cdot [L/(WC_iV_{ds})]$, where dI_{ds}/dV_{bg} is the maximum slope of the transfer curve under the linear coordinate; C_i is the capacitance of the gate layer; I_{ds} and V_{ds} are the drain- source current and voltage; and V_{bg} is the back gate voltage. The mobility of 12.5 $cm^2\ V^{-1}\ s^{-1}$ is extracted from the transfer curves of the MoS_2 FET with 3 μm channel length and a subthreshold swing of 468 mV dec^{-1} is obtained. After thermal annealing for the same MoS_2 FET, the effective electron mobility of 26.9 $cm^2\ V^{-1}\ s^{-1}$ is achieved, which is improved two-fold. The drain current on/off ratio is improved to 10^7 by one order of magnitude, and the subthreshold swing is reduced to 343 mV dec^{-1}. These results suggest that the thermal annealing process can effectively improve the performance of MoS_2 FETs in terms of all electrical parameters, which may be due to the improvement in the crystal quality of MoS_2 and the interface quality between MoS_2 and SiO_2, as well as metallization of metal/MoS_2 contacts. Similar results are also obtained for the other MoS_2 FETs with 0.5, 1, 2, 4 μm channel lengths before and after thermal annealing.

Figures 5(a) and (d) show current-voltage output characteristics (I_{ds}–V_{ds}) of MoS_2 FET with 3 μm channel length before and after thermal annealing at 300 °C for 2 h. There are two types of contact characteristics, as shown in figure 5(a). It is clearly shown in figure 5(b) that the super linear increase in drain current with no current saturation is observed for the MoS_2 FET when the gate voltage is above 0 V. As shown in figure 5(c), when the gate voltage is 0 V, as well as below that, the drain current has a non-linear relationship with the drain voltage, which is manifested as Schottky contacts. After the thermal annealing process, the drain current of the MoS_2 FET under positive gate bias increases linearly with the drain voltage, as shown in figure 5(e), while the non-linear relationship between the drain current and drain voltage is kept for the device under negative gate bias, as shown in figure 5(f).

To clarify the effect of thermal annealing, the output characteristics of the back-gated MoS_2 FETs before and after thermal annealing are compared under a gate voltage of 20 V, as shown in figure 6(a). The output characteristics can be divided into three regions for the MoS_2 FET before thermal annealing, as shown in figure 6(a). At the beginning, the drain current increases linearly with the drain voltage, labeled as region I. As the drain bias voltage increases, the drain current increases

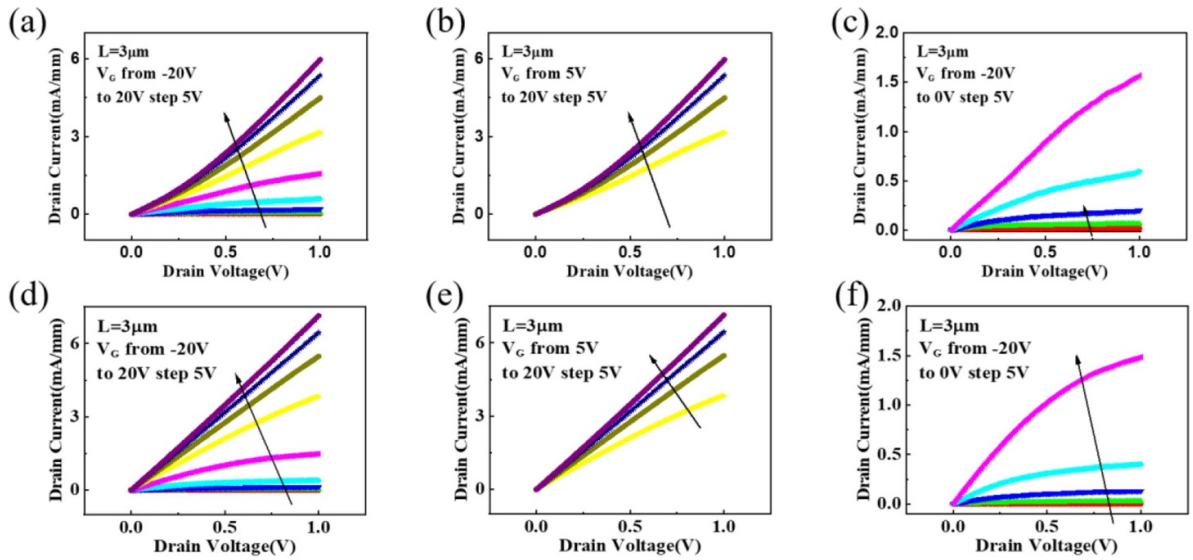

Figure 5. (a) Output characteristics of back-gated MoS_2 FET before thermal annealing under gate voltages from −20 V to 20 V. (b) Output characteristics of back-gated MoS_2 FET before thermal annealing under gate voltages from 5 V to 20 V. (c) Output characteristics of back-gated MoS_2 FET before thermal annealing under gate voltages from −20 V to 0 V. (d) Output characteristics of back-gated MoS_2 FET after thermal annealing under gate voltages from −20 V to 20 V. (e) Output characteristics of back-gated MoS_2 FET after thermal annealing under gate voltages from 5 V to 20 V. (f) Output characteristics of back-gated MoS_2 FET after thermal annealing under gate voltages from −20 V to 0 V.

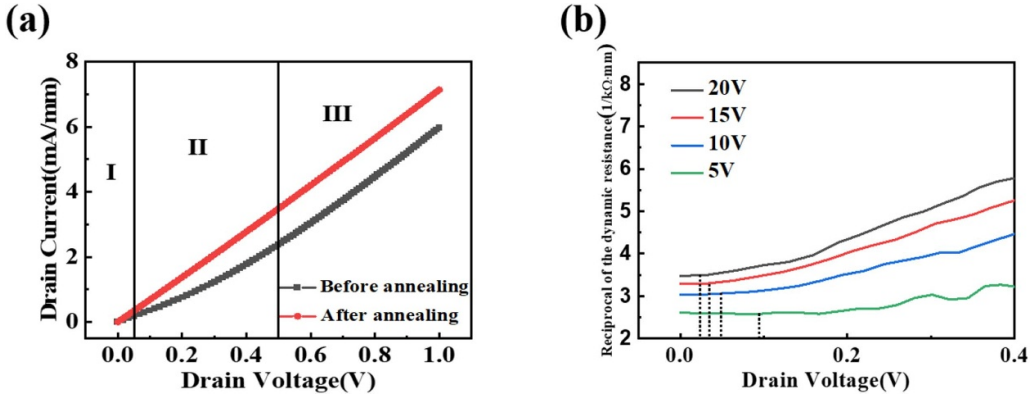

Figure 6. (a) Output characteristics of back-gated MoS_2 FET under the gate voltage of 20 V before and after annealing. (b) The extraction of the critical bias voltage under different gate voltages.

super linearly and the dynamic resistance decreases, labeled as region II. When continuing to increase the bias voltage, the drain current-voltage curve is almost parallel to that of the MoS_2 FET after thermal annealing, indicating that the dynamic resistance of the device before and after annealing is nearly equal, labeled as region III. Obviously, there is a critical voltage (V_C) when the linear relationship turns into a super linear relationship. We calculated the dynamic resistance to extract the critical voltage for the MoS_2 FET operating at gate bias from 20 V to 5 V, as shown in figure 6(b). The values of the critical voltage are also listed in table 2. The critical voltage increases with the decrease in the gate voltage, indicating that a higher gate voltage would make the change from linear to super linear occur more easily.

It is well known that the carrier concentration in the channel of MoS_2 FET should be fixed under a fixed gate voltage, rendering a constant sheet resistance. The decrease in the dynamic resistance with drain voltage from region I to region II implies that extra electrons should be excited to enlarge the current when the drain voltage is greater than the critical value. For the MoS_2 FETs before thermal annealing, the contact between Ti and MoS_2 without the metallization process cannot warrant complete formation of Ti–S covalent bonds [27]. The existence of the van de Waals gap at the contact interface between Ti and MoS_2 should be responsible for the higher dynamic resistance in region I. Meanwhile, S vacancies could introduce defect levels near the bottom of the conduction band in the basal plane and edges of mechanically

Table 2. The values of the critical voltage extracted from output characteristics before annealing.

V_G(V)	20	15	10	5
V_C(mV)	20	32	50	95

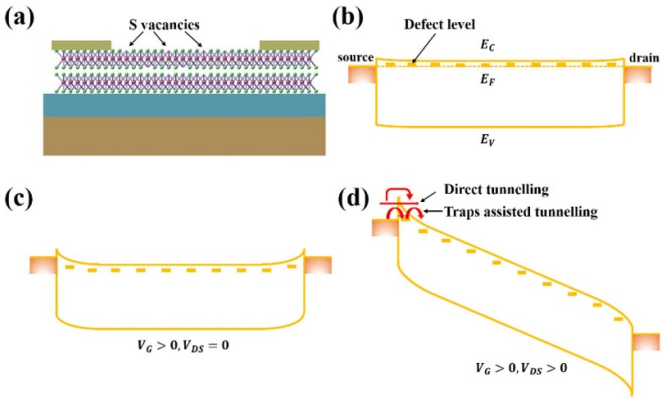

Figure 7. (a) A profile schematic image of the MoS_2 FET with S vacancies on the surface of MoS_2. (b) A band diagram of the MoS_2 FET with defect level. (c) A band diagram of the MoS_2 FET with positive gate voltage. (d) A band diagram of the MoS_2 FET with drain voltage.

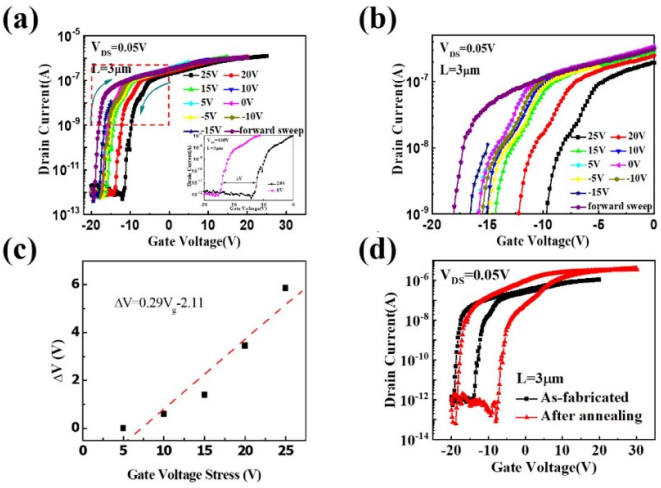

Figure 8. (a) Transfer characteristics of back-gated MoS_2 FET with 3 μm channel length at various gate bias stresses from 25 V to −15 V. (b) Local magnified transfer characteristics of the MoS_2 FET from figure 4(b) to emphasize the kinks. (c) Strong dependence of the transfer curve shift on gate bias stress. (d) Transfer characteristics and hysteresis for the MoS_2 FET before and after thermal annealing.

exfoliated MoS_2 [13]. The defect level assisted electron tunneling through the narrow contact barrier due to high accumulated electron density excessively increases the drain current with drain voltage, which might be the possible reason for the super linear increase in the drain current.

Figures 7(a) and (b) illustrate schematic images of the MoS_2 FET with S vacancies on the surface and band diagrams of the MoS_2 FET with defect levels. The contribution of defect level assisted tunneling to the total drain current is described in figures 7(c) and (d). After thermal annealing of the MoS_2 FET in vacuum at 300 °C, the metallization of Ti contacting with the MoS_2 layer is almost complete, leading to the disappearance of the van de Waals gap and the variation of the drain current relationship with drain voltage from a super linear to a linear increase. Meanwhile, the mechanism of defect level assisted electron tunneling loses efficacy due to the complete metallization of the contact interface of the MoS_2 layer.

Although the hysteresis of transfer curves of back-gated MoS_2 FETs has been investigated by several groups [21, 28–32], the explaination of the mechanism is still under debate. The intrinsic defects of S vacancies in MoS_2 was thought to play an important role besides some extrinsic factors, such as adsorption/desorption of gases on the unpassivated MoS_2 surface. However, the issues on the origin of the hysteresis are still open due to the complex situation in the fabrication of MoS_2 FETs. We measured the transfer curves of back-gated MoS_2 FET by gate voltage forward sweep from −20 V to 20 V and backward sweep with various sweep ranges, as shown in figures 8(a) and (b). The gate voltage stress is selected in the range 25 V to −15 V and all backward sweeping to −20 V. The transfer curves continuously shift to the right with the gate voltage stress changing from 0 V to 20 V, and an almost negligible change is observed when considering the test errors with the gate voltage stress changing from 0 V to −15 V. These results indicate that the transfer curve shift should be attributed to trapping and de-trapping of electrons at the defect trap centers near the MoS_2/SiO_2 interface when the status of the MoS_2 FET changes from accumulation to depletion modes. The dependence of the transfer curve shift ΔV on the basis of the 0 V gate voltage transfer curve at the drain current of 10^{-11} A on gate voltage stress is shown in figure 8(c). The transfer curve shift ΔV increases almost linearly with the positive gate voltage stress with the slope of 0.29. The strong dependence of the shift on gate voltage stress also suggests that the traps near the interface of MoS_2/SiO_2, rather than intrinsic defects in bulk or on the surface of MoS_2, play a critical role.

With respect to the MoS_2 FETs working in the 'on-state' with positive gate voltage at the beginning, electrons accumulate in the MoS_2 channel and raise the Fermi-level energy, thus trap centers near the MoS_2/SiO_2 interface should be filled. When the gate voltage sweeps from positive to negative, the MoS_2 channel begins to be depleted and the electrons de-trap from the trap centers, rendering the shift of the transfer curves.

It is interesting that the backward sweep transfer curves show kinks at the on/off inflection point, while no kinks are observed in the forward sweep transfer curves. This is a classical hump effect in the thin-film transistors, which has been reported by several groups [33–36]. Under a positive gate stress, a trend of bidirectional shift was revealed in the transfer characteristics. When the transfer characteristics shift towards the positive direction under a positive gate stress, the hump has a trend of negative shift. It has been proved that there are parasitic transistors connected in parallel with the main transistor in this single device, which is also the reason for the existence of the hump. The parasitic transistors are caused by the carriers trapping at the edge (edge effects) [35] or surface (backchannel) [36] of the MoS_2 flake. However, due to a lack of evidence, the origin of the hump in this device needs further investigation.

After thermal annealing, the transfer curves of the MoS_2 FET are also measured and are shown in figure 8(d). The observed difference in the hysteresis in this figure is due to the different gate voltage stress, which is consistent with the

relationship shown in figure 8(c). Hence, the hysteresis effect of the transfer curves has no obvious improvement by thermal annealing. This result indicates that the origins for the transfer curve shift and super linear increase in the drain current are different, although both may be defect traps. The former is the traps near the interface between MoS_2 and SiO_2, while the latter is the defects caused by S vacancies on the surface or in the bulk of MoS_2. It is concluded that thermal annealing in vacuum could improve the contact quality of MoS_2 and Ti; however, it will have no strong impact on defects at the interface between MoS_2 and SiO_2.

4. Conclusion

In summary, a TLM structure containing five back-gated MoS_2 FETs with various channel lengths was fabricated with metal Ti as contact electrodes. The specific contact resistivity and the resistivity of the MoS_2 channel are extracted from the TLM model, which are both sharply affected by the gate voltage due to the regulating effect on the carrier concentration of the gate voltage. The super linear increase in the drain current for the MoS_2 FETs is observed only at positive gate bias, which is attributed to the defect levels caused by S vacancies on the surface or in bulk of the MoS_2 flakes, which are removed by thermal annealing in vacuum. On the other hand, the traps at the interface between MoS_2 and SiO_2 are supposed to be the main origin of the hysteresis of the transfer curves of MoS_2 FETs, which is slightly affected by thermal annealing. These results further enrich the knowledge of the complex electrical characteristics of MoS_2 field-effect transistors to help us realize high performance MoS_2 FETs.

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